PATENT
8733.750.00-US

UNITED STATES PATENT APPLICATION

OF

SANG-HYUK LEE

FOR

ARRAY SUBSTRATE FOR IPS MODE LIQUID CRYSTAL DISPLAY DEVICE

McKenna Long & Aldridge, LLP
1900 K Street, N.W.
Washington, D.C. 20006
Tel: (202) 496-7500
Fax: (202) 496-7756

[0001] This application claims the benefit of Korean Patent Application No. 2001-87522, filed on December 28, 2001 in Korea, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a liquid crystal display (LCD) device and more particularly, to an array substrate for In-Plane Switching (IPS) mode liquid crystal display device which displays superior images by preventing light leakage in an area adjacent to a thin film transistor region.

Discussion of the Related Art

[0003] A typical liquid crystal display (LCD) device uses optical anisotropy and polarization properties of liquid crystal molecules. The liquid crystal molecules have a definite orientation order in alignment resulting from their thin and long shapes. The alignment direction of the liquid crystal molecules can be controlled by supplying an electric field to the liquid crystal molecules. In other words, as the alignment direction of the electric field is changed, the alignment of the liquid crystal molecules also changes. Because incident light is refracted to the orientation of the liquid crystal molecules due to the optical anisotropy of the aligned liquid crystal molecules, image data is displayed.

[0004] Active matrix liquid crystal display (AMLCD) devices, in which the thin film transistors and the pixel electrodes are arranged in the form of a matrix, are widely used because of their high resolution and superiority in displaying moving images. An array

substrate for the in-plane switching (IPS) mode liquid crystal display (LCD) device will be described hereinafter with reference to the following figures.

[0005] FIG. 1 is a plan view of a pixel of an array substrate for a related art in-plane switching (IPS) mode liquid crystal display (LCD) device. In FIG. 1, a plurality of gate lines 12 and common lines 16 are horizontally formed on an array substrate 10 and are spaced apart from each other. A plurality of data lines 24 is vertically formed on the array substrate 10 and cross the gate lines 12 and the common lines 16. The data line 24 defines a pixel region "P" by crossing the gate line 12. A thin film transistor "T" is formed at a crossing point of the gate line 12 and the data line 24. The thin film transistor "T" includes a gate electrode 14, an active layer 20, a source electrode 26 and a drain electrode 28. The gate electrode 14 communicates with the gate line 12 and the source electrode 26 communicates with the data line 24. The source electrode 26 has a U-shape surrounding the drain electrode 28 and the drain electrode 28 has an I-shape. A pixel electrode 30 that communicates with the drain electrode 28 and a common electrode 17 parallel with the pixel electrode 30 are formed in the pixel region "P". The common electrode 17 communicates with the common line 16. The pixel electrode 30 comprises an extension portion 30a, a vertical portion 30b and a horizontal portion 30c. The extension portion 30a of the pixel electrode 30 is extended from the drain electrode 28 and the vertical portion 30b of the pixel electrode 30 is vertically extended from the extension portion 30a. The horizontal portion 30c of the pixel electrode 30 is formed over the common line 16 and connects the vertical portions 30b into one portion. The common electrode 17 comprises a horizontal portion 17a and a plurality of vertical portions 17b. The plurality of the vertical portions 17b of the common electrode 17 is arranged in an alternating order with the vertical portions 30b of the pixel electrode 30. The

horizontal portion 17a of the common electrode 17 connects the plurality of the vertical portions 17b into one portion. The vertical portions 17b of the common electrode 17 are spaced apart from the data line 24. A storage capacitor "C" is formed in the pixel region "P". The storage capacitor "C" uses a portion of the common line 16 as a first storage electrode and the horizontal portion 30c of the pixel electrode 30 as a second storage electrode.

[0006] A typical driving method of a pixel will be described hereinafter with reference to FIG. 2 which is a signal graph illustrating voltage signals of a gate electrode and a common electrode during a frame. The graph shows applying states of a gate voltage (V_g) and a common voltage (V_{com}) during a frame period. In FIG. 2, V_{gh} and V_{gl} show a high and a low state of the gate voltage V_g and V_{dh} respectively, and V_{dl} show a high and a low state of the data voltage V_d. As shown in the figure, a voltage of about +18 volts is applied when the gate voltage (V_g) is in the on state and a voltage of about - 5 volts is applied when the gate voltage (V_g) is off state. A high-level data voltage (V_d) is inputted when the gate voltage (V_g) is in the on state and maintained until a next gate voltage (V_g) reaches the on state. This voltage applying process fulfills a drive of liquid crystal in the pixel region. If the liquid crystal display (LCD) device is normally black mode, a black color is displayed when the voltage is not applied. However, a light leakage phenomenon occurs in region "A" of FIG. 1 when the gate voltage (V_g) is in the off state.

[0007] FIG. 3 is a plan view illustrating an electric field direction between the gate electrode and the common electrode when the gate voltage (V_g) is in the off state according to the related art. FIG. 4 is a plan view illustrating an alignment direction of liquid crystal molecules between the gate electrode and the common electrode when the gate voltage (V_g) is in the off state according to the related art.

[0008] In FIG. 3, region "B" shows an electric field distribution in a region "E" between the gate electrode 14 and the common electrode 17. In FIG. 4, region "F" is a long axis direction of the liquid crystal 19 and region "D" is a rubbing direction of a substrate. As shown in FIG. 4, the liquid crystal 19 is aligned parallel with the rubbing direction when the voltage is not applied. However, an electric potential difference actual exists in the region "A" between the gate electrode 14 and the common electrode 17. Subsequently, the electric field distribution occurs, which has a certain direction, between the gate electrode 14 and the common electrode 17. As shown in FIG. 3 and FIG. 4, the electric field direction is perpendicular to the long axes "F" of the liquid crystal 19 in the region between the gate electrode 14 and the common electrode 17. The liquid crystal 19 will subsequently align according to the electric field direction when the gate voltage (V_g) is in the off state. Accordingly, light irradiated from a backlight passes through the "A" region and thus the light leakage phenomenon occurs when the gate voltage (V_g) is not applied at the normally black mode. Though a black matrix is generally formed on an upper substrate (not shown) in order to intercept the light leakage in the region "A", it still may be difficult to display a high quality image if an aligning error of the upper and lower substrate occurs.

SUMMARY OF THE INVENTION

[0009] Accordingly, the present invention is directed to an array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device that substantially obviates one or more of problems due to limitations and disadvantages of the related art.

[0010] An advantage of the present invention is to provide the array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device in order to display a high quality image by preventing light leakage in a region between a gate electrode and a common electrode.

[0011] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0012] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device comprises a gate line and a common line in a horizontal direction on a substrate; a data line crossing the gate line and the common line; a pixel electrode and a common electrode; and a thin film transistor at a crossing point of the gate line and the data line, the thin film transistor having a gate electrode, an active layer and source and drain electrodes, the gate electrode having a slope that satisfies a numeral expression $|\theta_R - \theta_g| = 89° \sim 91°$ (degrees), wherein θ_R is an angle of a rubbing direction measured from an arbitrary horizontal line and θ_g is an angle of the slope of the gate electrode measured from the arbitrary horizontal line. The common electrode and the pixel electrode are formed in a zigzag pattern. The source and drain electrodes are formed over a portion of the gate line. The source electrode has an U-shape and the drain electrode is formed in an interior of the U-shape.

[0013] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0015] In the drawings:

[0016] FIG. 1 is a plan view of a pixel of an array substrate for a related art in-plane switching (IPS) mode liquid crystal display (LCD) device;

[0017] FIG. 2 is a signal graph illustrating voltage signals of a gate electrode and a common electrode during a frame;

[0018] FIG. 3 is a plan view illustrating an electric field direction between the gate electrode and the common electrode when a gate voltage (V_g) is in the off state according to the related art;

[0019] FIG. 4 is a plan view illustrating an alignment direction of liquid crystal molecules between the gate electrode and the common electrode when a gate voltage (V_g) is in the off state according to the related art;

[0020] FIG. 5 is a plan view of a pixel of an array substrate for an in-plane switching (IPS) mode liquid crystal display (LCD) device according to a first embodiment of the present invention;

[0021] FIG. 6 is a plan view illustrating an electric field direction between a gate electrode and a common electrode according to the first embodiment of the present invention;

[0022] FIG. 7 is a graph illustrating angles of a rubbing direction and a slope of the gate electrode measured from a horizontal line; and

[0023] FIG. 8 is a plan view of a pixel of an array substrate for an in-plane switching (IPS) mode liquid crystal display (LCD) device according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0024] Reference will now be made in detail to embodiments of the present invention, example of which is illustrated in the accompanying drawings.

[0025] FIG. 5 is a plan view of a pixel of an array substrate for an in-plane switching (IPS) mode liquid crystal display (LCD) device according to a first embodiment of the present invention. In FIG. 5, a plurality of gate lines 112, common lines 116 and data lines 124 are formed on an array substrate 100 for in-plane switching (IPS) mode liquid crystal display (LCD) device. The gate line 112 and the common line 116 are formed in a horizontal direction and spaced apart from each other. The data line 124 crosses the gate line 112 and the common line 116 and defines a pixel region "P" by crossing the gate line 112. A thin film transistor "T" is formed at a crossing point of the gate and data lines. The thin film transistor

"T" has a gate electrode 114, an active layer 120 and source and drain electrodes 126 and 128. The gate electrode 114 communicates with the gate line 112 and the source electrode 126 communicates with the data line 124. The source electrode has an U-shape surrounding the drain electrode 128 and the drain electrode 128 has an I-shape. These shape of the source and drain electrodes 126 and 128 help to improve a mobility of an electron by shortening a channel length and widening a channel width between the source and drain electrodes 126 and 128. The gate electrode 114 has a slope of over about ninety degrees. A pixel electrode 130 and a common electrode 117 are formed in the pixel region "P". The pixel electrode 130 communicates with the drain electrode 128. The common electrode 117 communicates with the common line 116. The pixel electrode 130 has an extension portion 130a, a plurality of vertical portions 130b and a horizontal portion 130c. The extension portion 130a is extended from the drain electrode 128. The vertical portions 130b are vertically extended from the extended portion 130a and spaced apart from each other. The horizontal portion 130c is disposed over the common line 116 and connects the plurality of vertical portions 130b into one portion. The common electrode 117 has a plurality of vertical portions 117b and a horizontal portion 117a. The vertical portions 117b are vertically extended from the common line 116 and arranged in an alternating pattern with the vertical portions 130b of the pixel electrode 130. The horizontal portion 117a connects the vertical portions 117b into one portion. The horizontal portion 117a of the common electrode 117 has a side that is parallel with the slope of the gate electrode 114. The slope of the gate electrode 114 is perpendicular to a rubbing direction "G". Under this structure of the common electrode and the gate electrode, an electric field direction "H" and the rubbing direction "G" become parallel to

each other between the common electrode 117 and the gate electrode 114 when a gate voltage is in the off state.

[0026] FIG. 6 is a plan view illustrating an electric field direction between a gate electrode and a common electrode according to the first embodiment of the present invention. In FIG. 6, only the gate line 112, the gate electrode 114 and the common electrode 117 are illustrated. As shown in the figure, because an alignment direction of liquid crystal 119 is parallel with the electric field direction "H" between the common electrode 117 and the gate electrode 114, there is no change in alignment direction of the liquid crystal 119 from an initial alignment state. Accordingly, there is no change in a polarization of light that passes through a region between the common electrode 117 and the gate electrode 114 so that clearer black mode can be displayed. That is, because an electric potential difference does not occur between the common electrode 117 and the gate electrode 114, a light leakage phenomenon does not occur.

[0027] The common electrode 117 and the gate electrode 114 can be designed as follows. In FIG. 7, θ_R is an angle measured from a horizontal line "J" to the rubbing direction "G" and θ_g is an angle measured from the horizontal line "J" to the slope 114a of the gate electrode 114. The common electrode 117 and the gate electrode 114 can be designed using a formula as follows:

$$|\theta_R - \theta_g| = 89° \sim 91° \text{ (degrees)}$$

[0028] An array substrate for in-plane switching (IPS) mode liquid crystal display (LCD) device according to a second embodiment of the present invention, which is designed using the above formula, will be explained hereinafter with reference to FIG. 8.

[0029] FIG. 8 is a plan view of a pixel of an array substrate for an in-plane switching (IPS) mode liquid crystal display (LCD) device according to the second embodiment of the present invention. As shown in FIG. 8, a plurality of gate lines 212, common lines 216 and data lines 224 are formed on an array substrate 200. The gate lines 212 and the common lines 216 are formed in a horizontal direction and spaced apart from each other. The data line 224 crosses the gate line 212 and the common line 216 and defines a pixel region "P" by crossing the gate line 212. A thin film transistor "T" is formed at a crossing point of the gate and data lines 212 and 224. The thin film transistor "T" has a gate electrode 214, an active layer 220 and source and drain electrodes 226 and 228. The gate electrode 214 communicates with the gate line 212 and the source electrode 226 communicates with the data line 224. The source electrode 226 has an U-shape surrounding the drain electrode 228. The drain electrode 228 has an I-shape. As a result of this structure of the source and drain electrodes 226 and 228, a channel length can be shortened and a channel width can be widened between the source electrode 226 and the drain electrode 228, and thus a mobility of an electron can be improved. A pixel electrode 230 and a common electrode 217 are formed in the pixel region "P". The pixel electrode 230 communicates with the drain electrode 228 and the common electrode 217 communicates with the common line 216. The common electrode 217 is formed parallel to the pixel electrode 230. The pixel electrode 230 has an extension portion 230a, a plurality of vertical portions 230b and a horizontal portion 230c. The extension portion 230a is extended from the drain electrode 228. The vertical portions 230b are vertically extended from the common line 216. The horizontal portion 230c is disposed over the common line 216 and connects the vertical portions 230b into one portion. The common electrode 217 has a plurality of vertical portions 217b that is formed in an alternating pattern with the vertical

portions 230b of the pixel electrode 230. A rubbing direction "K" is perpendicular to the gate electrode 214. In this structure, when a gate voltage is in the off state, an electric field direction "L" and an alignment direction of liquid crystal between the gate electrode 214 and the common and pixel electrodes 217b and 230b is parallel with the rubbing direction "K". Accordingly, a black mode can be displayed clearly because there is no change in the alignment direction of the liquid crystal from an initial state.

[0030] Though the embodiments illustrated here are for normally black mode, these embodiments may be applied to normally white mode. That is, a white color can be displayed clearly by forming the electric field direction and the alignment direction of liquid crystal between the gate electrode and the common electrode when the gate voltage is in the off state.

[0031] The present invention newly designs a gate electrode and a common electrode in order to make an initial alignment direction of liquid crystal parallel with an electric field direction between the gate electrode and the common electrode.

[0032] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.